NX-422 EXERCISE 3 – Implantable Circuits Solutions

1. OTAs have a larger g_m.

(a) The gain of the inverting amplifier:

Since g_m is large, we can assume the negative input of the OTA is grounded (equal to the positive input of the OTA). So we can write a KCL at that node:

$$-\frac{\mathbf{V_{in}}}{\boldsymbol{R_{in}}} - \frac{\boldsymbol{V_{out}}}{\boldsymbol{R_f}} = \mathbf{0}$$

$$\frac{\boldsymbol{V_{out}}}{\boldsymbol{V_{in}}} = -\frac{\boldsymbol{R_f}}{\boldsymbol{R_{in}}}$$

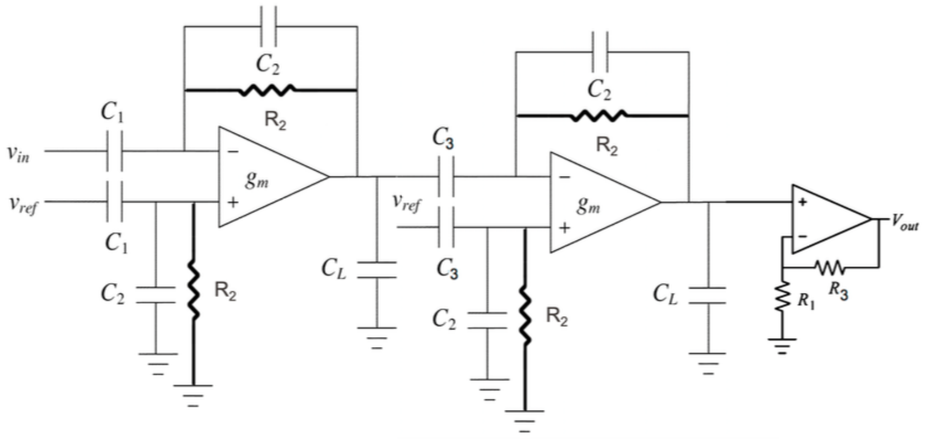
(b) The gain of the non-inverting amplifier:

Since g_m is large, we can assume the negative input of OTA is equal to the positive input of the OTA. So we can write a KCL at that node:

$$\frac{\mathbf{V_{in}}}{\boldsymbol{R_1}} + \frac{\boldsymbol{V_{in}} - \boldsymbol{V_{out}}}{\boldsymbol{R_2}} = \mathbf{0}$$

$$\frac{\boldsymbol{V_{out}}}{\boldsymbol{V_{in}}} = \frac{\boldsymbol{R_1} + \boldsymbol{R_2}}{\boldsymbol{R_1}}$$

2. Let’s check the details of the three-stage neural amplifier.



(a) The equation for the overall mid-band gain:

$$|\mathbf{A_V}|_{\mathbf{3-Stage}} = |\mathbf{A_{V1}} \times \mathbf{A_{V2}} \times \mathbf{A_{V3}}| = \left(\frac{\mathbf{C_1}}{\mathbf{C_2}}\right) \times (\frac{\mathbf{C_3}}{\mathbf{C_2}}) \times (\frac{\mathbf{R_1} + \mathbf{R_3}}{\mathbf{R_1}})$$

(b) Assuming $C_2 = C_u$, we will find the values of C_1 and C_3 in terms of C_u. Ignore C_L, and assume R_1=40kΩ and R_3=60kΩ. For our calculations, we are asked to have a total mid-band gain of 1000 and minimize the chip area by minimizing the total capacitance.

Let's start:

$\mathbf{C_2 = C_u}$ assume $\mathbf{C_1 = M \times C_u}$ and $\mathbf{C_3 = N \times C_u}$

We know that R_1=40kΩ and R_3=60kΩ. Hence, $\frac{\mathbf{R_1+R_3}}{\mathbf{R_1}} = \frac{\mathbf{100k\Omega}}{\mathbf{40k\Omega.}} = \mathbf{2.5.}$

$$|\mathbf{A_V}|_{\mathbf{3-Stage}} = \mathbf{1000} \rightarrow \left(\frac{C_1}{C_2}\right) \times \left(\frac{C_3}{C_2}\right) = \frac{\mathbf{1000}}{\mathbf{2.5}} = \mathbf{400} = \mathbf{M \times N}$$

Total capacitance excluding C_L is

$$= \mathbf{2C_1 + 2C_2 + 2C_3 + 2C_2 = 2 \times (M + N + 2) \times C_u}$$

Area $\propto \mathbf{2 \times (M + N + 2) \times C_u}$

$$\mathbf{2 \times (M + N + 2) \times C_u = 2 \times \left(M + \frac{400}{M} + 2\right) \times C_u} = \boldsymbol{f(M)}$$

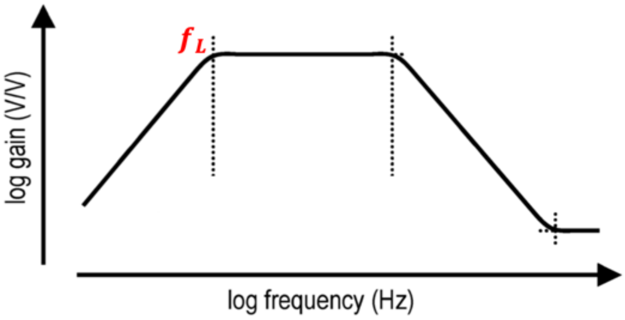
To minimize the total capacitance and area $\frac{\boldsymbol{df}}{\boldsymbol{dM}} = \mathbf{0} \rightarrow \mathbf{1 - \frac{400}{M^2} = 0}$

$\rightarrow \mathbf{M_{opt} = 20}$

$\rightarrow \mathbf{C_1 = 20}\boldsymbol{C_u}$ and $\mathbf{C_3} = \frac{\mathbf{400}}{\mathbf{20}}\boldsymbol{C_u} = \mathbf{20}\boldsymbol{C_u}$

(c) To locate the low-frequency limit and high-frequency limit, we need to analyze the pole frequency at each relevant node to determine which one is dominant. We need to calculate each of them one by one, as it's not always obvious just from looking at the schematic.

In our example, we are told that the amplifier's bandwidth is set by the first stage, and $C_2 = 400\text{fF}$.



$$\mathbf{f_L = \frac{1}{2 \times \pi \times R_2 \times C_2} = 1\ Hz}$$

$$\mathbf{C_2 = C_u = 400\ fF}$$

$$\mathbf{R_2 = \frac{1}{2 \times \pi \times 400 \times 10^{-15}} = 3.98 \times 10^{11} = 0.398\ T\Omega}$$

3. We will draw the drain current of an NMOS ($\mathrm{I_D}$) as a function of $\mathrm{V_{GS}}$ where $\mathrm{V_{GS}}$ varies from $0 \rightarrow 3\mathrm{V}$.

- $\frac{W}{L} = \frac{50}{0.5}, V_{DS} = 3\ V, V_{TH} = 0.7\ V,\ \mu_n C_{ox} = 50\ \mu A/V^2$

(a) Saturation condition: $\mathbf{V_{DS} > V_{GS} - V_{TH}}$

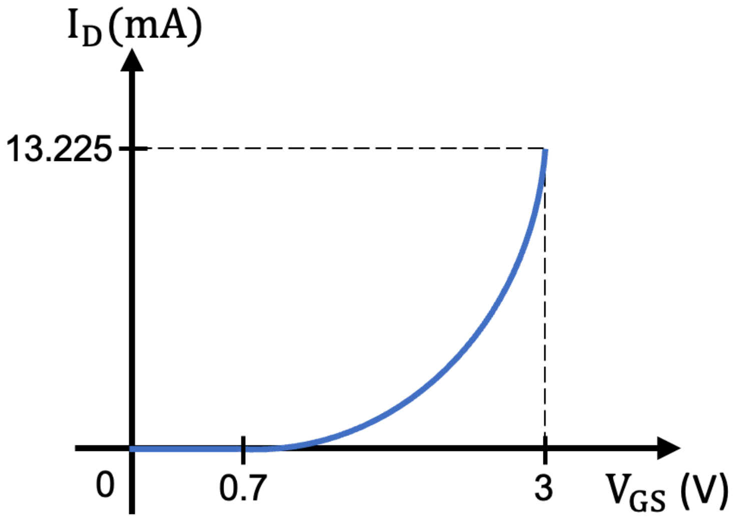
$3V > (0 \rightarrow 3V) - 0.7V$, which means that the assumption is correct. The transistor is in saturation.

The drain current equation for the saturation:

$$\mathbf{I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2}$$

$$I_D = \frac{1}{2} \times \left(50\frac{\mu A}{V^2}\right) \times \frac{50}{0.5} \times (V_{GS} - 0.7)^2 = 2.5\frac{mA}{V^2}(V_{GS} - 0.7)^2$$

At $\mathbf{V_{GS} = 3V \rightarrow I_D = 13.225mA}$



(b) If V_{DS} = 1V,

- For V_{GS}-V_{TH} < V_{DS}, the transistor is in the saturation region.
- For V_{GS}-V_{TH} > V_{DS}, the transistor is in triode region.

V_{GS} - 0.7 < 1 ⟶ V_{GS} < 1.7 ⟶ I_D = same as before: $\mathbf{I_D} = \frac{1}{2}\boldsymbol{\mu_n C_{ox}} \frac{\mathbf{W}}{\mathbf{L}}(\mathbf{V_{GS}} - \mathbf{V_{TH}})^2$

V_{GS} - 0.7 > 1 ⟶ V_{GS} > 1.7 ⟶ $\mathbf{I_D} = \boldsymbol{\mu_n C_{ox}} \frac{\mathbf{W}}{\mathbf{L}}[(\mathbf{V_{GS}} - \mathbf{V_{TH}})\mathbf{V_{DS}} - \frac{1}{2}\mathbf{V_{DS}^2}]$

Replacing V_{DS} = 1 in the equation, we have: $\mathbf{I_D} = (\mathbf{50}\,\frac{\boldsymbol{\mu}\mathbf{A}}{\mathbf{V^2}}) \times \frac{\mathbf{50}}{\mathbf{0.5}} \times [(\mathbf{V_{GS}} - \mathbf{0.7}) - \frac{1}{2}]$